IN THE SPECIFICATION

Following is a marked-up version of each amended paragraph of the subject patent application. The Examiner is requested to delete the indicated paragraph and replace it with the amended paragraph.

Replace paragraph **[0027]** with the following:

[0027] Figure 11 illustrates an embodiment of an inductor 89 comprising a conductive element 90 in the same metallization layer as the conductive lines 66A, for extending the terminal end 76. In this embodiment the void 82 is larger than in the embodiment of Figure 9, thus increasing ~~lowering~~ the Q factor of the inductor 89, when compared with the inductor 71 of Figure 9.

Replace paragraph **[0028]** with the following:

[0028] Figure 12 is a plan view of the inductor 89 ~~71~~ of Figure 11, with the cross-sectional view of Figure 11 taken along the plane 11-11 of Figure 12.

Replace paragraph **[0029]** with the following:

[0029] Figure 13 is a cross-sectional view of an inductor 92, wherein both terminal ends 76 are spaced apart from the inductor 71 to allow the formation of a larger void 82 than present in the embodiments described heretofore. To form this embodiment an intermetallic dielectric layer 94 is disposed over the conductive lines 66A, and a second metallization layer overlying the intermetallic dielectric layer 94 comprises a conductive element 98 formed therein. A tungsten plug 100 connects the terminal end 76 to the conductive element 98. A tungsten plug 102 connects the conductive line 98 to an active region in the substrate 10. With both terminal ends 76 connected to an active region outside the footprint of the inductor 92~~71~~, the void 82 can encompass substantially the entire region below the inductor 92.

Replace paragraph **[0034]** with the following:

[0034] Prior to formation of the intermetallic dielectric layer 144 voids are formed in regions 150, underlying the inductor 120, using conventional masking, patterning and etching

steps. The voids are filled with silicon dioxide (a dielectric material) or another relatively low loss material prior to formation of the intermetallic dielectric layer 144 thereover. In another embodiment (not shown in Figure 14) a region of the substrate 122 below the inductor 120 is also removed, according to the teachings above. ~~above.~~ As in the previous embodiment, the absence of semiconductor and metallization layers below the inductor 120 reduces eddy current loses and improves the inductor Q factor.